Notice of References Cited	Application/Control No. 09/751,930	Applicant(s)/Patent Under Reexamination WANG ET AL.	
	Examiner CHAMELI C DAS	Art Unit 2122	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,119,222	09-2000	Shiell et al.	712/238
	B	US-5,974,538	10-1999	Wilmot, II, Richard Byron	712/218
	C	US-5,537,669	07-1996	Evans et al.	382/141
	D	US-5,999,737	12-1999	Srivastava, Amitabh	717/162
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	TITLE: Instruction issue logic for high-performance, interruptable pipelined processor, author: Sohi et al, ACM, 1987.
	V	TITLE: Synthesis of Pipelined Instruction Set processors, author: Cloutier et al, ACM, 1993.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.